Operational Amplifier

The operational amplifier (OP-Amp) is a common device in audio-frequency (AF) and radio-frequency (RF) amplifier applications. OP-Amp is a direct-coupled amplifier with very high voltage gain, very high input impedance and very low output impedance. It is usable in the frequency range from 0 to a few MHz. It is also designed to perform mathematical operations such as summation, subtration, differentiation, integration etc in analog computer. That is why it is called operational amplifier. A large variety of OP-Amp are available almost in Integrated Circuits (IC).

IC741 is commercially available OP-Amp. It is a 8-pin chip. The op-Amp packages contain single or dual (two) or quad (four) op-Amp in a single IC. The pin diagram of single op-Amp IC741 is shown in Fig-1 (a) and its circuit symbol is shown in Fig-1(b).

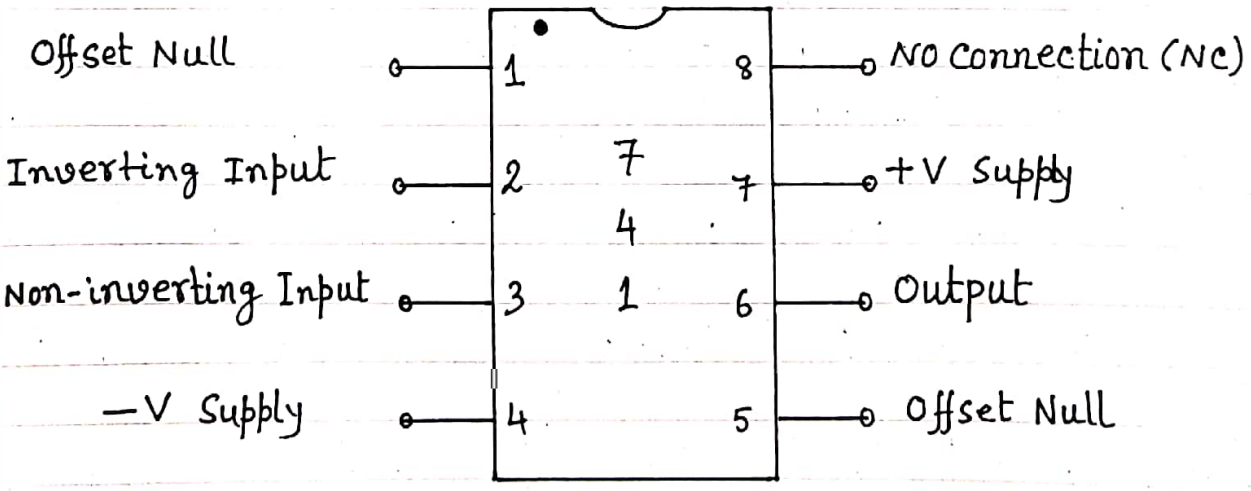


Fig-1(a)

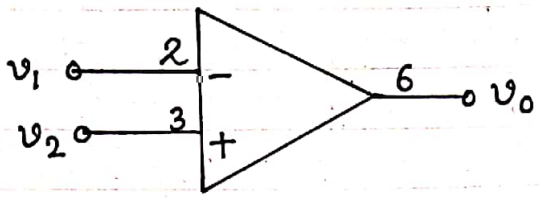


Fig-1(b).

Characteristics of Ideal Op-Amp :-

An ideal op-Amp has the following characteristics:

1. Open-loop voltage gain is infinite ($A = \infty$)
2. Input resistance R_i is infinite ($R_i = \infty$)
3. Output resistance R_o is zero ($R_o = 0$
4. Bandwidth is infinite ($BW = \infty$). Therefore, any frequency signal from 0 to ∞ Hz can be amplified without attenuation.
5. Perfect balance i.e, output is zero when two input voltages are equal
6. Characteristics do not drift with temperature.
7. Common Mode Rejection Ratio (CMRR) is infinite.
8. Infinite Slew Rate ($SR = \infty$). Therefore, output voltage changes occur simultaneously with input voltage changes.

In practice, the above characteristics of op-Amp can never be realised. The practical op-Amp can be made close to ideal values as given in Table-I

Property	Ideal	Practical	Typical Value
open-loop gain	infinite	Very High	2×10^5
Input resistance	infinite	High	$2\,M\Omega$
Output resistance	Zero	Low	$75\,\Omega$
CMRR	infinite	High	90 dB
Bandwidth	infinite	Very High	2 MHz

Equivalent Circuit of an op-Amp:

An equivalent circuit of an op-Amp with finite input and output resistances is shown in Fig-2

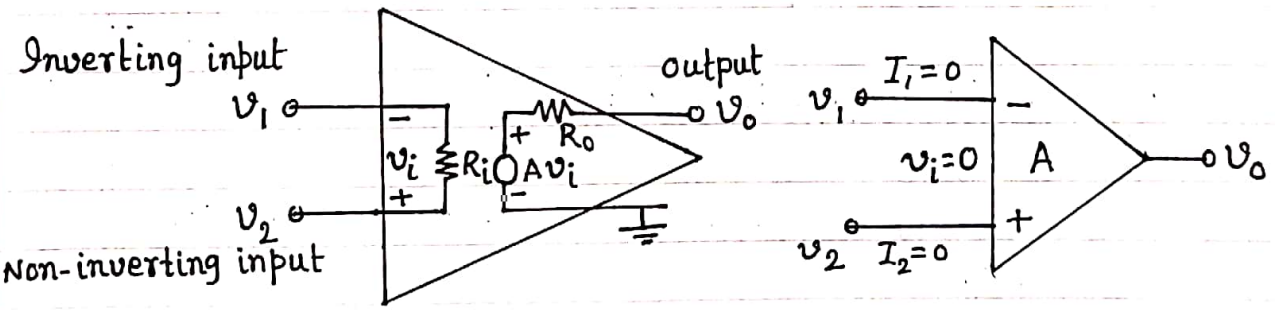


Fig-2

The output voltage v_o can be expressed as $v_o = A(v_2 - v_1) = Av_i$
Therefore, the output voltage v_o is directly proportional to the difference between v_2 and v_1 or the op-Amp amplifies the difference between two input voltages.

Ideal Voltage Transfer Curve of Op-Amp :

The basic op-Amp equation $v_o = A v_i = A(v_2 - v_1)$ is justified when the output offset voltage is assumed to be zero. The ideal voltage transfer curve of op-Amp is shown in Fig-3. It is clear from Fig-3 that the output voltage cannot exceed the positive saturation voltage $+V_{sat}$ (+ve supply of op-Amp) and negative saturation voltage $-V_{sat}$. (-ve supply of op-Amp).

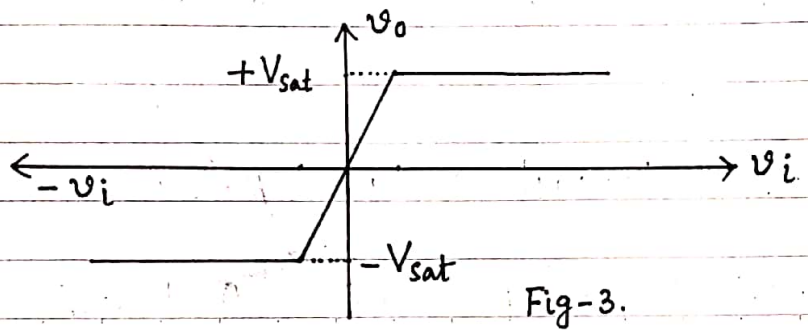


Fig-3.

Differential Amplifier and Common Mode Rejection Ratio (CMRR) :

The block diagram of a typical op-Amp is shown in Fig-4.

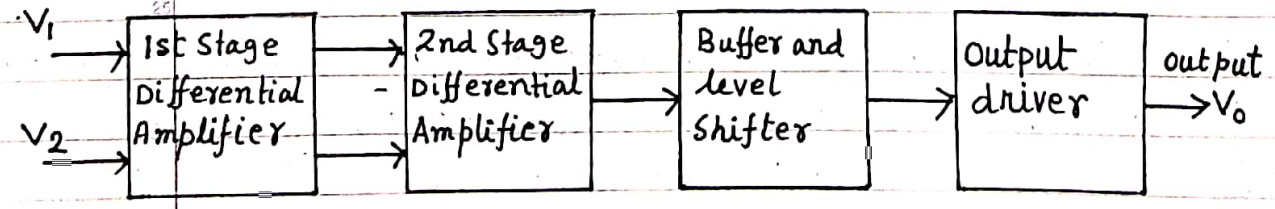
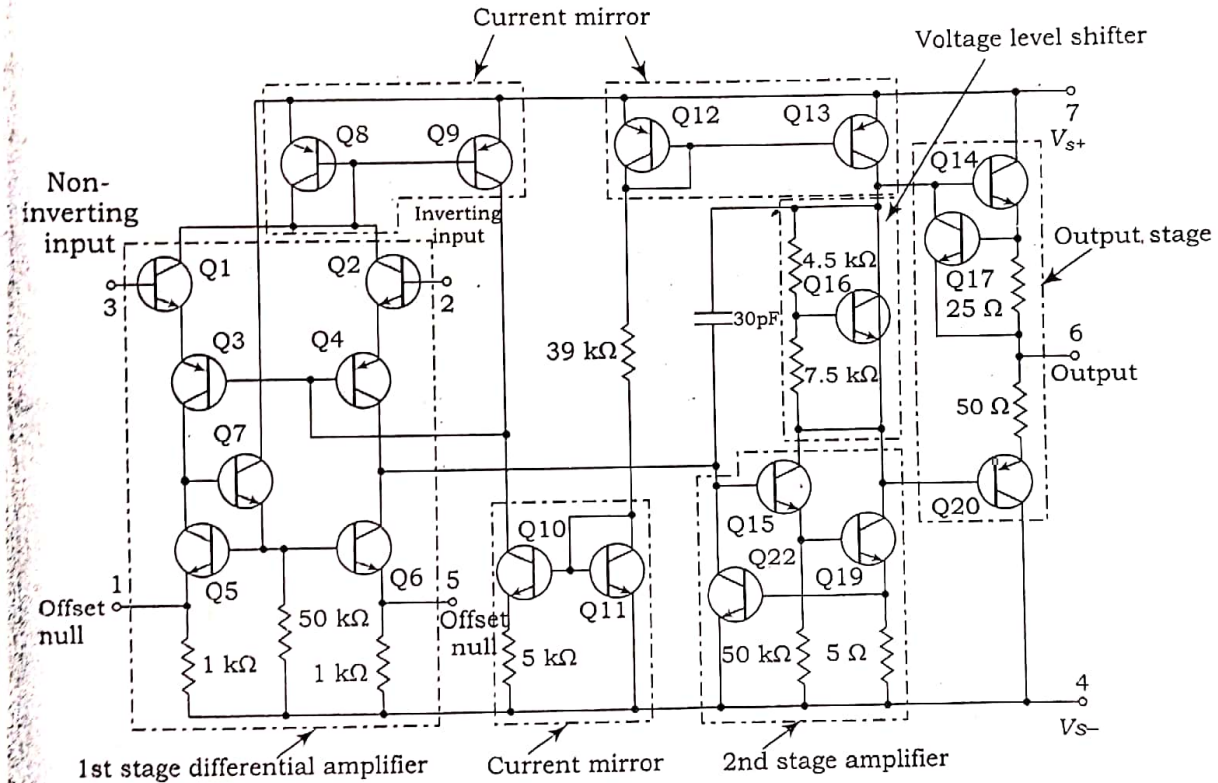


Fig-4

The first two stages are cascaded differential amplifiers

which are used to provide high gain and high input resistance Actually, the buffer is an emitter-follower. Its input impedance is very high. Hence, it prevents loading of the high gain stage. The level shifter adjusts the d.c voltages and the output voltage is zero for zero inputs. The emitter-follower circuit in the third-stage is also used to provide low output resistance.

Fig-5 shows the internal circuit of a 741 Op-Amp.



Internal circuit diagram of 741 OP-AMP Fig-5

The basic circuit at the input stage of an op-Amp is a differential amplifier which amplifies the difference of two input signals. Thus if v_1 and v_2 are the inputs applied to the inverting and non-inverting terminals respectively then the output v_o of ideal op-Amp is given by

$$v_o = A_d (v_2 - v_1) = A_d v_d$$

where A_d is the gain for the difference signal $v_d = v_2 - v_1$. Therefore if $v_1 = v_2$ then $v_o = 0$. But in practical Op-Amp this is not the case because the output depends not only on the difference signal $v_d = v_2 - v_1$ but also upon the average level $v_c = \frac{v_1 + v_2}{2}$, called the common mode signal. For example, output with $v_2 = 10\mu V$, $v_1 = -10\mu V$ and that with $v_2 = 110\mu V$, $v_1 = 90\mu V$ will be different though the difference, $v_2 - v_1 = 20\mu V$ in both the cases. This happens due to lack of perfect circuit symmetry. Thus, in general

$$v_o = A_d v_d + A_c v_c$$

$$= A_d v_d \left[1 + \frac{A_c}{A_d} \cdot \frac{v_c}{v_d}\right]$$

$$= A_d v_d \left[1 + \frac{1}{\frac{A_d}{A_c}} \cdot \frac{v_c}{v_d}\right]$$

$$= A_d v_d \left[1 + \frac{1}{CMRR} \cdot \frac{v_c}{v_d}\right]$$

where A_c is the voltage gain for common mode signal. The Common Mode Rejection Ratio (CMRR) is defined as

$$CMRR = \left|\frac{A_d}{A_c}\right|$$

It serves as a figure of merit of a differential amplifier. Higher is the value of CMRR better is the performance of the amplifier. Being a large value CMRR is sometimes expressed in dB:

$$CMRR\,(dB) = 20 \log_{10} \left|\frac{A_d}{A_c}\right|$$

IC 741 Op-Amp has a CMRR of about 90 dB.

Fig-6 shows the basic circuit of an emitter coupled differential amplifier. The two transistors (Q_1 and Q_2) and the collector resistors R_c are taken to be identical. Ideally both the transistors should have the same operation-point. Thus perfect symmetry exists between two halves of the circuit. With $v_1 = v_2$, $I_{c1} = I_{c2} = I/2$ (neglecting base circuits). Keeping v_2 fixed if v_1 is increased a large fraction of the fixed current is diverted into Q_1. Hence V_{o1} will fall and V_{o2} will rise. So voltage gain $A = \frac{\Delta V_{o1}}{\Delta v_1}$ will be negative (inverting) while the gain $\frac{\Delta V_{o2}}{\Delta v_1}$ will be positive (non-inverting).

Similarly $\frac{\Delta V_{o1}}{\Delta v_2} > 0$ and $\frac{\Delta V_{o2}}{\Delta v_2} < 0$. For perfectly symmetric circuit various gains must be equal or equal and opposite. when both v_1 and v_2 changes

$$\Delta V_{o1} = \left.\frac{\Delta V_{o1}}{\Delta v_1}\right|_{\Delta v_2 = 0} \cdot \Delta v_1 + \left.\frac{\Delta V_{o1}}{\Delta v_2}\right|_{\Delta v_1 = 0} \cdot \Delta v_2$$

$$= A(\Delta v_1 - \Delta v_2)$$

Similarly $\Delta V_{o2} = A(\Delta v_2 - \Delta v_1)$. Thus the circuit amplifies the difference of two input signals and acts as differential amplifier.

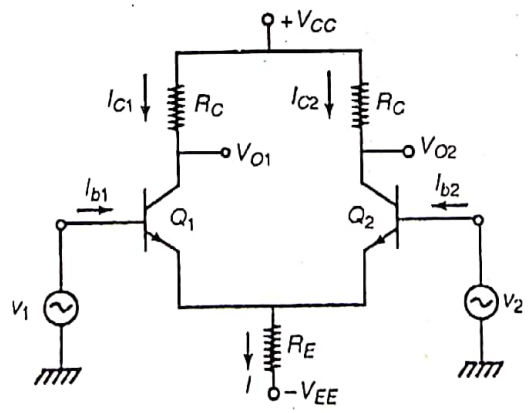


Fig. 6 An emitter coupled differential amplifier

Problem 1. The difference amplifier as shown in Fig-7 has the following parameters: $R_C = 10K\Omega$, $R_E = 100K\Omega$, $R_S = 10K\Omega$. The transistor parameters are as follows:

$h_{ie} = 10K\Omega$, $h_{fe} = 100$, $h_{re} = 0$, $h_{oe} = 0$

When the amlifier is operated with common-mode signal of 50 mV and difference signal of 25 mV, determine output voltage and CMRR.

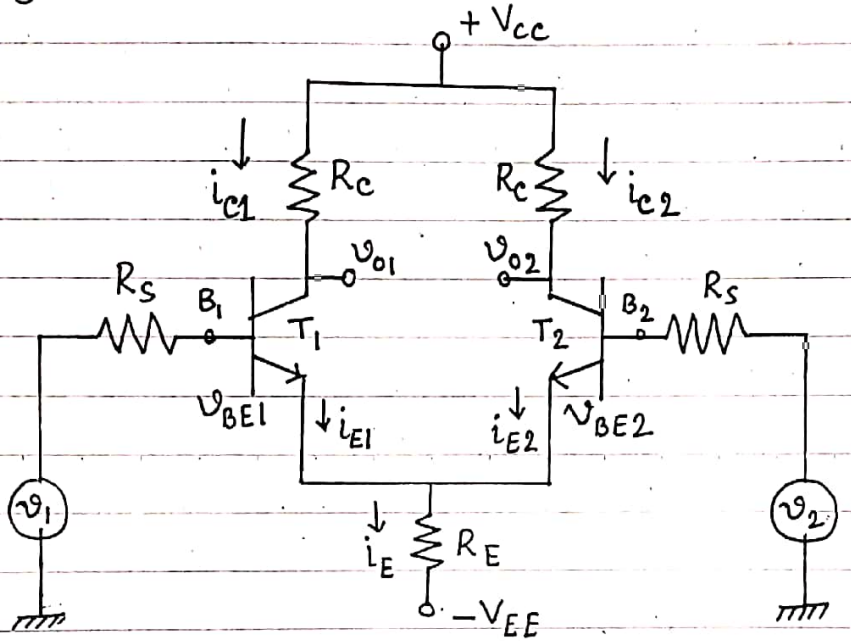


Fig-7

Solution: The difference gain is

$$A_d = -\frac{h_{fe} R_c}{2(R_s + h_{ie})} = -\frac{100 \times 10 \times 10^3}{2(10 \times 10^3 + 10 \times 10^3)}$$

$$= -\frac{100 \times 10 \times 10^3}{2 \times 2 \times 10 \times 10^3} = -25$$

The common-mode gain is

$$A_c = -\frac{h_{fe} R_c}{R_s + h_{ie} + (1 + h_{fe}) 2R_E} = -\frac{100 \times 10 \times 10^3}{10 \times 10^3 + 10 \times 10^3 + 2 \times 101 \times 100 \times 10^3}$$

$$= -0.0495$$

The output voltage $v_o = A_d v_d + A_c v_c$

$= (-25) \times 25mV + (-0.0495) \times 50\,mV$

$= -627.475\,mV.$

The common-mode rejection ratio in dB is

$$CMRR = 20 \log_{10}\left(\frac{A_d}{A_c}\right) = 20 \log_{10}\left(\frac{25}{0.0495}\right) = 54.06\,dB.$$

Problem 2. When the voltage $v_2 = +40\mu V$ is applied to the non-inverting input terminal and a voltage $v_1 = -40\mu V$ is applied to the inverting terminal of an op-Amp, an output $v_o = 100\,mV$ is obtained. But when $v_1 = v_2 = +40\mu V$, one obtain $v_o = 0.4\,mV$. Calculate the voltage gains for the difference and the common-mode rejection ratio.

Solution: In the first case, the difference signal is $v_d = v_2 - v_1 = 40 - (-40) = 80\mu V$ and the common-mode signal is $v_c = \frac{v_1 + v_2}{2} = \frac{-40+40}{2} = 0\,\mu V$

The output voltage is $v_o = A_d v_d + A_c v_c =$

For the first case

$$100 \times 10^{-3} = A_d \times 80 \times 10^{-6} + A_c \times 0$$

$$\therefore A_d = \frac{10^5}{80} = 1250$$

In the second case $v_d = v_2 - v_1 = 40 - 40 = 0\,\mu V$

$$v_c = \frac{v_1 + v_2}{2} = \frac{40+40}{2} = 40\,\mu V$$

The output voltage for the second case

$$0.4 \times 10^{-3} = A_d \times 0 + A_c \times 40 \times 10^{-6}$$

$$\therefore \quad A_c = \frac{0.4 \times 10^3}{40} = 10$$

The CMRR $= \left| \frac{A_d}{A_c} \right| = \frac{1250}{10} = 125$

In dB $\quad 20 \log_{10} 125 = 41.94$ dB.

Problem 3. The CMRR of a differential amplifier using op-Amp is 100 dB. The output voltage for a differential input 200 μV is 2V. Determine the common-mode voltage gain.

Solution: $\quad CMRR = 20 \log_{10} \left| \frac{A_d}{A_c} \right|$

$$A_d = \frac{2\,V}{200\,\mu V} = \frac{2 \times 10^6}{200} = 10^4$$

Now

$$\log_{10} \left| \frac{A_d}{A_c} \right| = \frac{100}{20} = 5$$

$$\therefore \quad \frac{A_d}{A_c} = 10^5 \quad \therefore A_c = \frac{A_d}{105} = \frac{10^4}{10^5} = \frac{1}{10} = 0.1$$

$$\therefore \boxed{A_c = 0.1}$$

Applications of Operational Amplifiers :

1. Inverting Amplifier using Op-Amp :

The basic inverting amplifier using Op-Amp is shown in Fig-1. Since the input resistance of the op-Amp is infinite, practically no current enters into the op-Amp. Therefore, current i through R_1 is also the current through R_2.

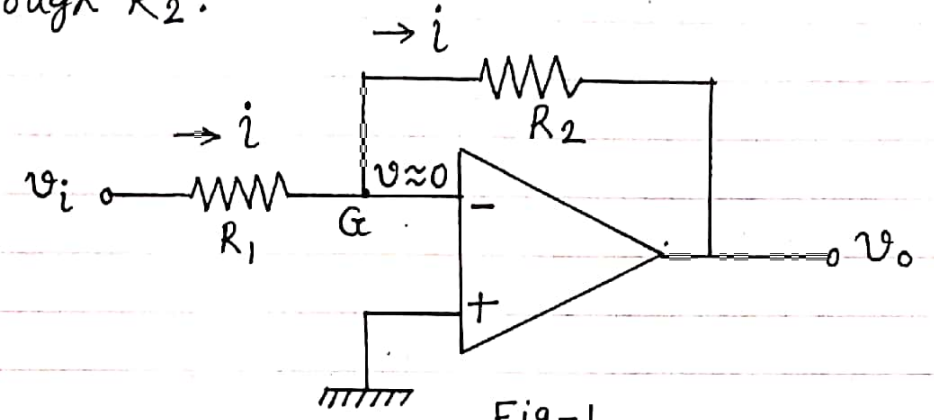


Fig-1.

$$\therefore\ i = \frac{v_i - v}{R_1} = \frac{v - v_o}{R_2} \quad \text{--------(1)}$$

Now since the open-loop gain $\frac{v_o}{v} = \alpha$, for a finite v_o, v must be zero i.e the point G is virtual ground point. The potential of G is zero but G is not directly connected to actual ground point. From (1) we get

$$i = \frac{v_i - 0}{R_1} = \frac{0 - v_o}{R_2} \quad \text{--------(2)}$$

So the close-loop voltage gain of the inverting amplifier is

$$\boxed{A_V = \frac{v_o}{v_i} = -\frac{R_2}{R_1}} \quad \text{--------(3)}$$

The negative sign indicates that the output is 180° out of phase with the input. The gain depends on the ratio of R_2 and R_1 and is independent of Op-Amp parameters.

1.1 Scale Changer:

In Fig-1 if R_1 and R_2 are two accurately known resistors then the output

$$v_o = -\frac{R_2}{R_1} v_i = -K v_i \quad \text{------ (1.1)}$$

where $K = R_2/R_1$ is a constant. Thus the circuit multiplies the input by $-K$, called the scale factor. Thus the circuit of Fig-1 can act as a scale changer

1.2 Phase Shifter:

In Fig-1 if R_1 and R_2 are replaced by impedances Z_1 and Z_2. Then as before

$$\frac{v_o}{v_i} = -\frac{Z_2}{Z_1} \quad \text{- - - - - - - - - - - - - - - (1.2)}$$

If Z_1 and Z_2 are taken to have equal magnitude but different phase then we can write

$$\frac{v_o}{v_i} = -\frac{|Z_2| e^{j\theta_2}}{|Z_1| e^{j\theta_1}} = e^{j(\pi + \theta_2 - \theta_1)} \quad \text{- - - - - - - (1.3)}$$

where θ_1 and θ_2 are respectively the phase angles of Z_1 and Z_2. Thus the op-Amp can shift the phase of input voltage v_i by the angle $(\pi + \theta_2 - \theta_1)$ which can have any value from 0° to 360°. So the circuit using op-Amp is used as phase-shifter circuit.

2. Non-inverting Amplifier using op-Amp :

The basic circuit of non-inverting amplifier using op-Amp is shown in Fig-2. The input signal v_i is applied at the non-inverting terminal. Now if v is the potential at the point A then the differential input $(v_i - v)$. So the output $v_o = A(v_i - v)$. Since A (open-loop gain) $= \infty$ for a finite v_o we must have $v = v_i$. Since the input impedance of the op-Amp is infinite practically no current enters into the op-Amp. So almost same current passes through R_1 and R_2. R_2 is the feedback resistor. Thus

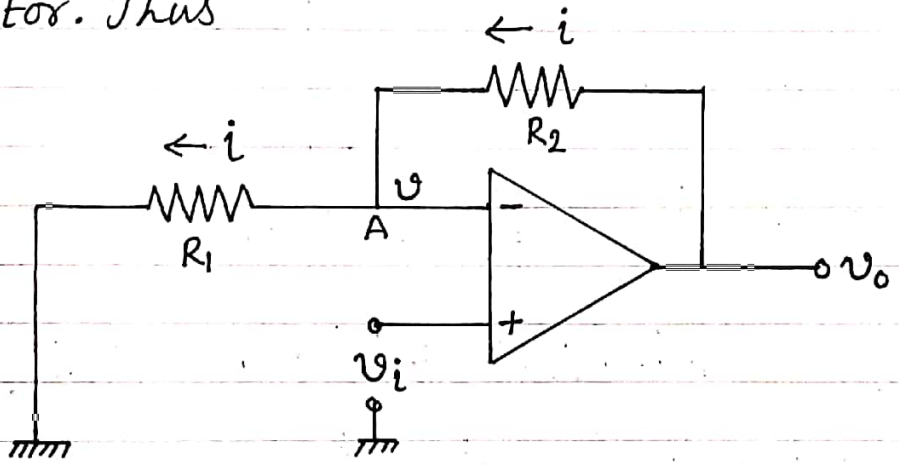


Fig-2

$$\frac{v_o - v}{R_2} = \frac{v - 0}{R_1}$$

$$\Rightarrow \frac{v_o - v_i}{R_2} = \frac{v_i}{R_1} \Rightarrow \frac{v_o}{v_i} = 1 + \frac{R_2}{R_1}$$

Thus close-loop voltage gain is

$$\boxed{A_V = \frac{v_o}{v_i} = 1 + \frac{R_2}{R_1}} \quad \text{----------(2.1)}$$

The output voltage v_o is in phase with v_i.

2.1 Unity Gain Buffer:

The close-loop voltage gain of a non-inverting amplifier using op-Amp is

$$A_V = \frac{v_o}{v_i} = 1 + \frac{R_2}{R_1} \quad \text{----------(2.1)}$$

It is found that $\frac{v_o}{v_i}$ becomes unity if we choose $R_1 = \infty$ and/or $R_2 = 0$. The amplifier (Fig-2.1) acts as a voltage follower or unity gain follower or unity gain buffer.

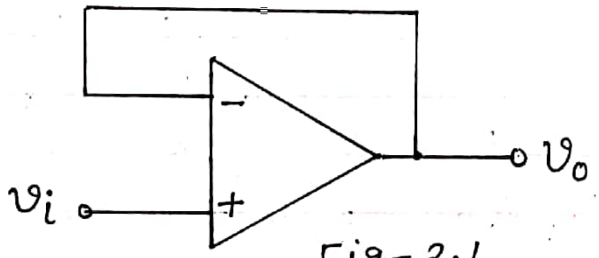


Fig-2.1

3. Adder or Summing Amplifier using op-Amp :

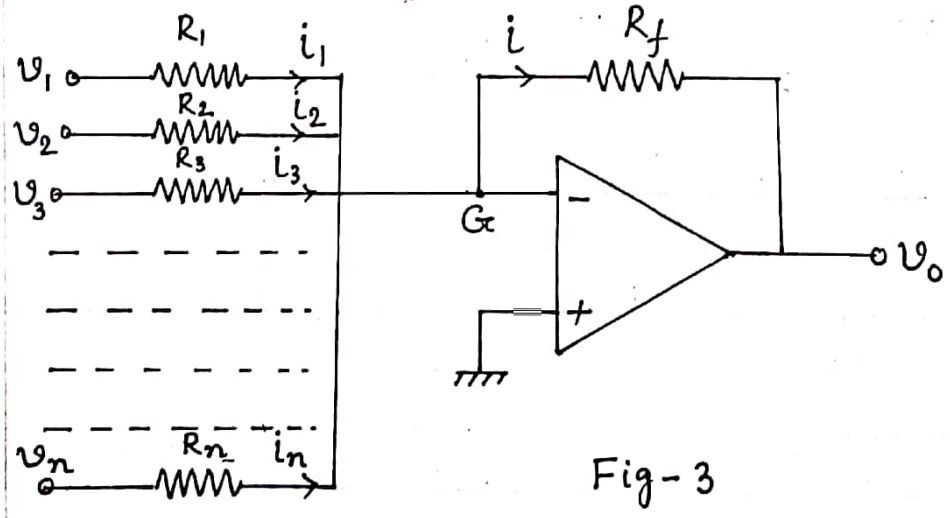


Fig-3

The adder or summing amplifier circuit using op-Amp is shown in Fig-3. Since the point G

is a virtual ground point and due to infinite input impedance of the op-Amp no current passes into the op-Amp. Then we can apply KCL at G we get

$$i = i_1 + i_2 + i_3 + \cdots + i_n$$

$$\Rightarrow -\frac{v_o}{R_f} = \frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} + \cdots + \frac{v_n}{R_n}$$

$$\Rightarrow v_o = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \frac{R_f}{R_3}v_3 + \cdots + \frac{R_f}{R_n}v_n\right)$$

If $R_1 = R_2 = R_3 = \cdots = R_n$ Then

$$v_o = -\frac{R_f}{R_1}(v_1 + v_2 + v_3 + \cdots + v_n)$$

R_f/R_1 is the gain of the summing amplifier. If $R_f = R_1$

$$\therefore v_o = -(v_1 + v_2 + v_3 + \cdots + v_n) \quad \text{---------- (3.1)}$$

4. Differential Amplifier using op-Amp :

The circuit diagram of a differential amplifier using op-Amp is shown in Fig-4.

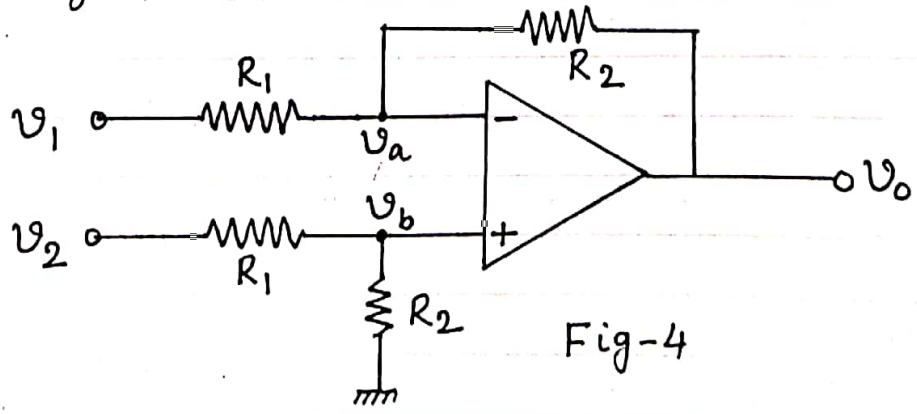


Fig-4

v_1 and v_2 are the inputs at the inverting and non-inverting terminals respectively. Since the open-loop gain and input impedance of the op-Amp are infinite, no current enters into the op-Amp. Therefore

$$\frac{v_1 - v_a}{R_1} = \frac{v_a - v_o}{R_2} \quad \text{----------(4.1)}$$

and $$\frac{v_2 - v_b}{R_1} = \frac{v_b - 0}{R_2} \quad \text{----------(4.2)}$$

Putting $v_a = v_b$ we get from (4.1) and (4.2)

$$\frac{v_1 - v_a}{R_1} = \frac{v_a - v_o}{R_2} \quad \text{----------(4.3)}$$

and $$\frac{v_2 - v_a}{R_1} = \frac{v_a}{R_2} \quad \text{----------(4.4)}$$

Subtracting (4.3) from (4.4) we get

$$\frac{1}{R_1}(v_2 - v_1) = \frac{v_o}{R_2}$$

$$\therefore v_o = \frac{R_2}{R_1}(v_2 - v_1) \quad \text{----------(4.5)}$$

If $R_1 = R_2$ then from equation (4.5) we get

$$v_o = (v_2 - v_1) \quad \text{----------(4.6)}$$

Thus the circuit acts as <u>Subtractor.</u>

5. Integrator Circuit using Op-Amp :

The circuit diagram of integrator using op-Amp is shown in Fig-5. The point G is the virtual ground point and its potential is zero.

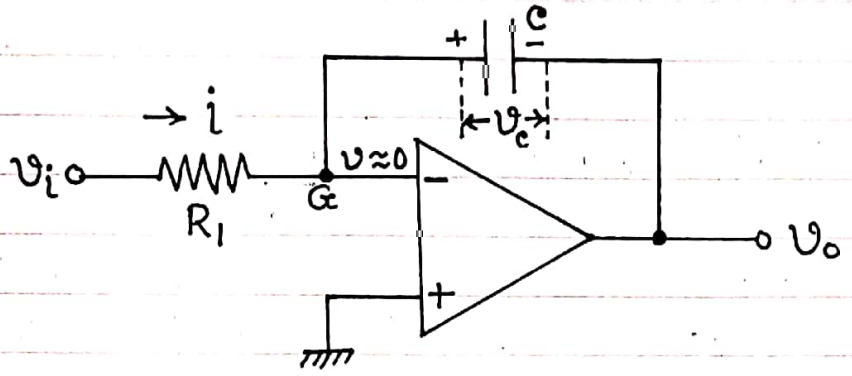


Fig-5

The current i flowing through R_1 is given by

$$i = \frac{v_i - 0}{R_1} = \frac{v_i}{R_1} \quad \text{---------- (5·1)}$$

The input impedance of the op-Amp is infinite, the current flows through the feedback Capacitor C to produce the output voltage v_o

The voltage developed across C is

$$v_c = \frac{1}{C}\int i\,dt = \frac{1}{CR_1}\int v_i\,dt \quad [\text{using (5·1)}]$$

Now $v_o + v_c = 0$

$$\therefore v_o = -v_c = -\frac{1}{CR_1}\int v_i\,dt$$

$$\therefore v_o = -\frac{1}{CR_1}\int v_i\,dt \quad \text{---------- (5·2)}$$

The equation (5·2) shows that the output voltage is the

integration of the input voltage v_i. That is $v_o \propto \int v_i dt$ and the proportionality constant is $(-1/CR_1)$.
If $R_1 = 1M\Omega$ and $C = 1\mu F$ then $\frac{1}{CR_1} = 1$ and

$$v_o = -\int v_i dt \quad \text{.....(5.3)}$$

5.1 Practical Integrator Circuit :

The basic integrator circuit (Fig-5) has the drawback that since the capacitor is an open circuit for d.c, the d.c voltage gain of the op-Amp circuit is infinite. So any d.c voltage at the input would drive the op-Amp output to saturation ($\pm V_{sat}$). To remove this problem a resistance R_2 is connected parallel to C which limits the d.c voltage gain of the amplifier. For proper operation of the integrator circuit $R_2 \gg \frac{1}{\omega C_2}$ where ω is the angular frequency of the input signal v_i. Thus the frequency of operation for proper integration $f = \omega/2\pi$ must be larger than the cut-off frequency $f_c = \frac{1}{2\pi C R_2}$. In this situation we choose $f > 10 f_c$ for integration of v_i. The practical integrator circuit is shown in Fig-5.1.

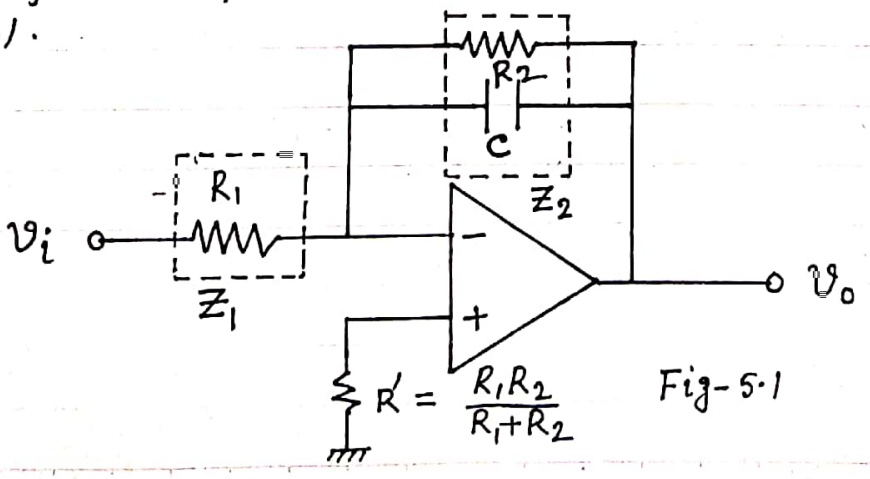


Fig-5.1

Circuit Analysis :

From the Fig-5·1, $Z_1 = R_1$ and

$$\frac{1}{Z_2} = \frac{1}{R_2} + j\omega C = \frac{1+j\omega C R_2}{R_2}$$

$$\therefore Z_2 = \frac{R_2}{1+j\omega C R_2}$$

The close-loop voltage gain of the circuit of Fig-5·1 is given by

$$A_V = -\frac{Z_2}{Z_1} = -\frac{R_2/R_1}{(1+j\omega C R_2)}.$$

Now
$$|A_V| = \frac{R_2/R_1}{\sqrt{1+\omega^2 C^2 R_2^2}}$$

The variation of $|A_V|$ with ω is shown in Fig-5·2

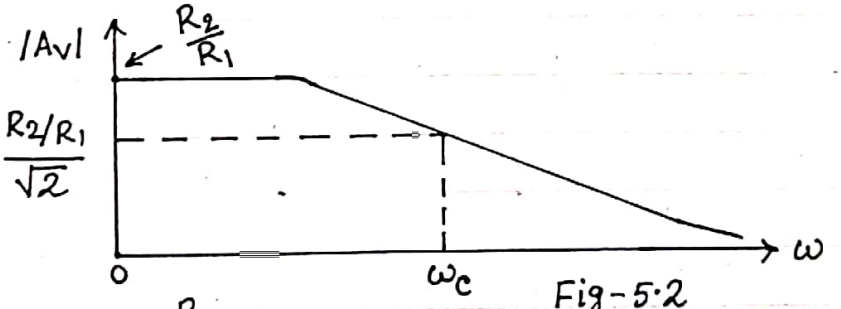


Fig-5·2

At $\omega = \omega_c$, $|A_V| = \frac{R_2/R_1}{\sqrt{2}}$

$$\therefore \frac{R_2}{R_1\sqrt{2}} = \frac{R_2/R_1}{\sqrt{1+\omega_c^2 C^2 R_2^2}}$$

$$\therefore \sqrt{1+\omega_c^2 C^2 R_2^2} = \sqrt{2} \quad \therefore \omega_c = \frac{1}{CR_2} \quad \therefore \boxed{f_c = \frac{1}{2\pi C R_2}}$$

6. Differentiator Circuit using op-Amp

The differentiator circuit using op-Amp is shown in Fig-6. The point G is the virtual ground point because of the infinite gain of the op-Amp. The potential at the point G is zero.

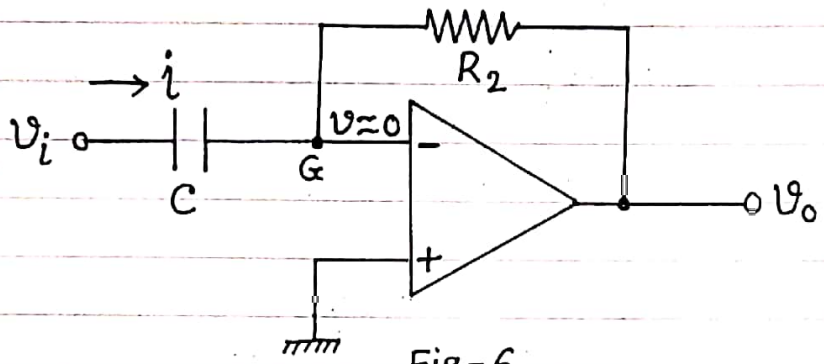


Fig-6

The charge on the Capacitor C at any instant of time t is

$$q = C v_i$$

$$\therefore v_i = \frac{q}{C}$$

Differentiating w.r.to t we have

$$\frac{dv_i}{dt} = \frac{1}{C}\frac{dq}{dt} = \frac{i}{C} \quad \text{--------(6.1)}$$

where i is the current flowing through the Capacitor C. Since the input impedance of the op-Amp is infinite, the current i flows through the feedback resistance R_2. Therefore

$$i = \frac{v - v_o}{R_2} = -\frac{v_o}{R_2}$$

Putting the value of i into equation (6.1) we get

$$\frac{dv_i}{dt} = -\frac{1}{CR_2} v_o$$

$$\therefore v_o = -CR_2 \frac{dv_i}{dt} \quad \text{----------(6.2)}$$

The equation (6.2) shows that the output voltage v_o is proportional to the time derivative of the input voltage v_i. The proportionality constant is $(-CR_2)$. Let $C = 1\mu F$ and $R_2 = 1M\Omega$

$$v_o = -\frac{dv_i}{dt} \quad \text{----------(6.3)}$$

6.1 Practical Differentiator Circuit :

The practical differentiator circuit using Op-Amp is shown in Fig-6.1

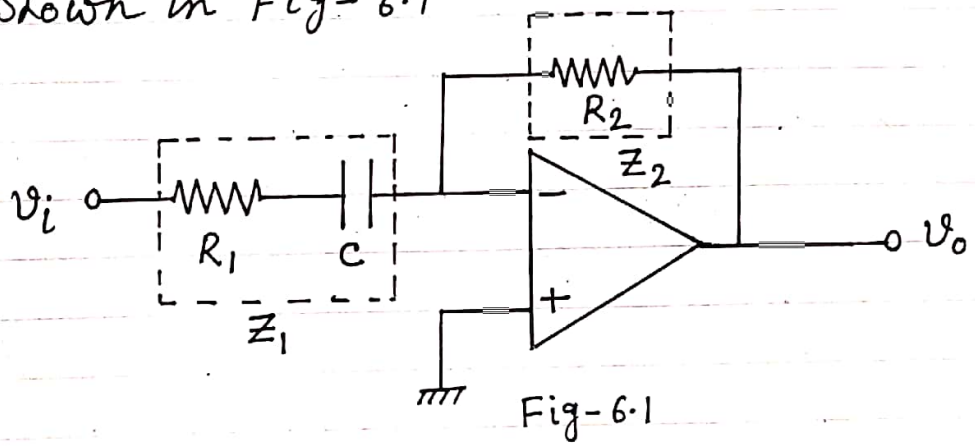


Fig-6.1

Circuit Analysis :

In Fig-6.1, $Z_2 = R_2$ and $Z_1 = R_1 + \frac{1}{j\omega C} = \frac{1 + j\omega CR_1}{j\omega C}$

The close-loop voltage gain of the circuit of Fig-6.1

$$A_V = -\frac{Z_2}{Z_1} = -\frac{R_2}{\frac{1+j\omega CR_1}{j\omega C}}$$

$$= -\frac{j\omega CR_2}{1+j\omega CR_1}$$

$$= -\frac{j\omega CR_2(1-j\omega CR_1)}{(1+j\omega CR_1)(1-j\omega CR_1)}$$

$$= -\frac{\omega^2C^2R_1R_2 + j\omega CR_2}{(1+\omega^2C^2R_1^2)}$$

$$= -\left[\frac{\omega^2C^2R_1R_2}{(1+\omega^2C^2R_1^2)} + j\frac{\omega CR_2}{(1+\omega^2C^2R_1^2)}\right]$$

$$\therefore |A_V| = \left|\frac{v_o}{v_i}\right| = \left[\left(\frac{\omega^2C^2R_1R_2}{(1+\omega^2C^2R_1^2)}\right)^2 + \left(\frac{\omega CR_2}{(1+\omega^2C^2R_1^2)}\right)^2\right]^{1/2}$$

$$= \left[\frac{\omega^2C^2R_2^2 + (\omega^2C^2R_1R_2)^2}{(1+\omega^2C^2R_1^2)^2}\right]^{1/2}$$

$$= \left[\frac{\omega^2C^2R_2^2(1+\omega^2C^2R_1^2)}{(1+\omega^2C^2R_1^2)^2}\right]^{1/2}$$

$$= \left[\frac{\omega^2C^2R_2^2}{1+\omega^2C^2R_1^2}\right]^{1/2} \text{-------(6.4)}$$

At very low frequency $\omega CR_1 << 1$ and we neglect ωCR_1 and the equation (6.4) becomes

$$\therefore |A_v| = \left| \frac{v_o}{v_i} \right| = \omega C R_2 = 2\pi f C R_2$$

At very high frequency $\omega C R_1 >> 1$ we neglect 1 and the equation (6.4) becomes

$$|A_v| = \left| \frac{v_o}{v_i} \right| = \frac{R_2}{R_1}$$

The variation of $|A_v|$ with ω is shown in Fig-6.2

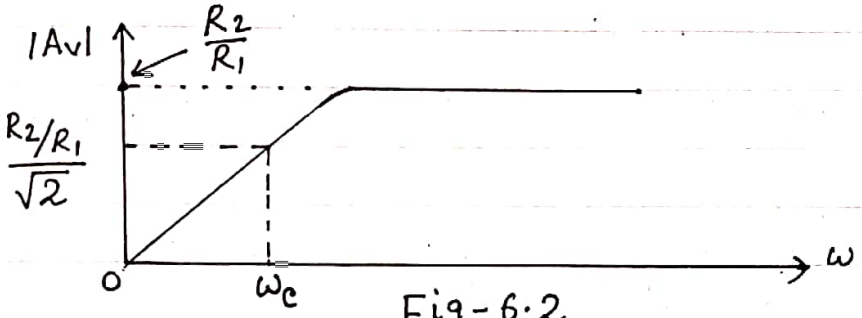


Fig-6.2

From the equation (6.4)

$$\frac{\frac{R_2}{R_1}}{\sqrt{2}} = \left[\frac{\omega_c^2 C^2 R_2^2}{1 + \omega_c^2 C^2 R_1^2} \right]^{1/2} = \frac{\omega_c C R_2}{\sqrt{1 + \omega_c^2 C^2 R_1^2}}$$

$$\Rightarrow \sqrt{(1 + \omega_c^2 C^2 R_1^2} = \sqrt{2}\, \omega_c C R_1$$

$$\Rightarrow (1 + \omega_c^2 C^2 R_1^2) = 2 \omega_c^2 C^2 R_1^2$$

$$\Rightarrow \omega_c^2 C^2 R_1^2 = 1 \Rightarrow \omega_c = \frac{1}{CR_1}$$

$$\therefore \boxed{f_c = \frac{1}{2\pi C R_1}}$$

6.2 Integrator and differentiator circuit using R and C:

The R-C low pass filter or R-C integrator circuit is shown in Fig-6.3. The R-C high pass filter or R-C differentiator circuit is shown in Fig-6.4

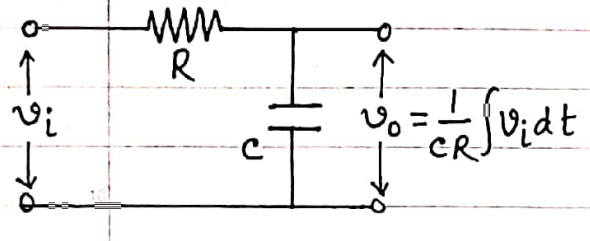


Fig-6.3

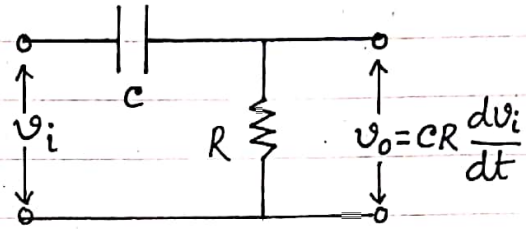


Fig-6.4

Problem 4: Find the expression of output voltage of the following circuit of Fig-4

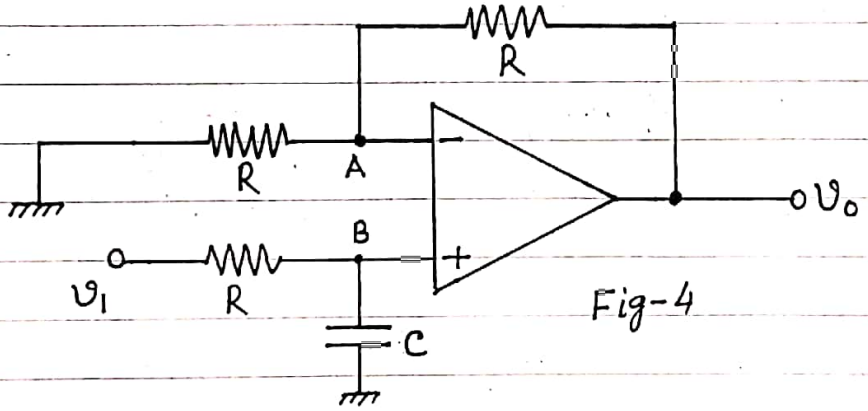


Fig-4

Solution: The potential at the point B is

$$v_B = \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} v_1 = \frac{1}{1 + j\omega CR} v_1 = v_A$$

The output voltage of the non-inverting amplifier using Op-Amp is

$$v_0 = \left(1+\frac{R}{R}\right)v_B = 2v_B$$

$$= \frac{2}{1+j\omega CR}v_1$$

At high frequency $j\omega CR >> 1$

$$\therefore v_0 \approx \frac{2}{j\omega CR}v_1 = \frac{2}{CR}\int v_1 dt \quad \because \frac{1}{j\omega} = \int dt.$$

This circuit acts as non-inverting integrator.

Problem 5 Find the expression of the output voltage of the circuit of Fig-5

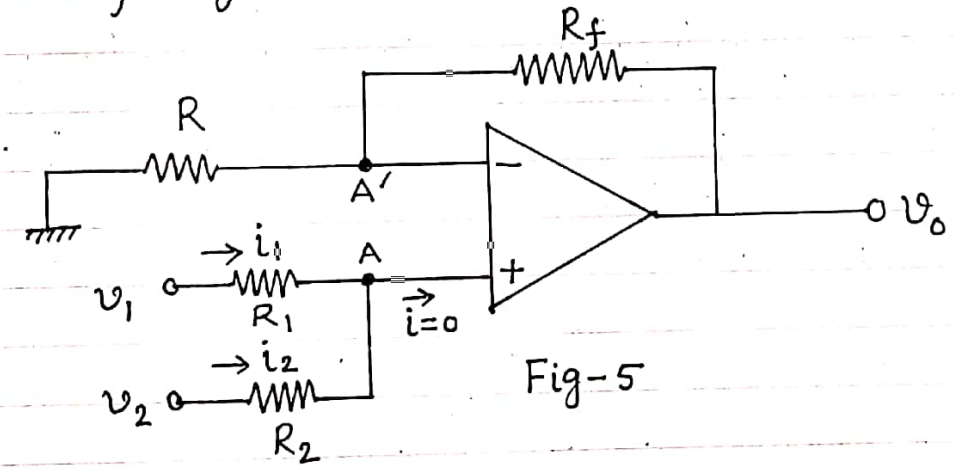


Fig-5

Solution: Applying KCL at node A we can write

$$i_1 + i_2 = i = 0$$

$$\therefore \frac{v_1 - v_A}{R_1} + \frac{v_2 - v_A}{R_2} = 0$$

$$\Rightarrow \frac{v_1}{R_1} + \frac{v_2}{R_2} = v_A\left(\frac{1}{R_1}+\frac{1}{R_2}\right) \quad \therefore v_A = \frac{\frac{v_1}{R_1}+\frac{v_2}{R_2}}{\left(\frac{1}{R_1}+\frac{1}{R_2}\right)}$$

The output voltage of the non-inverting amplifier with resistors R_1 and R_f is

$$v_o = \left(1 + \frac{R_f}{R}\right) v_A$$

$$= \left(1 + \frac{R_f}{R}\right)\left[\frac{\frac{v_1}{R_1} + \frac{v_2}{R_2}}{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)}\right]$$

If $R_1 = R_2 = R_f = R$ $\boxed{v_o = v_1 + v_2}$

This circuit acts as non-inverting adder circuit.

7. Current to voltage Converter :

The current to voltage converter circuit using op-Amp is shown in Fig-7. The output is proportional to the input current. No current passes through R_s. Whole current passes through R, therefore

$$v_o = -i_s R \quad \therefore v_o \propto -i_s$$

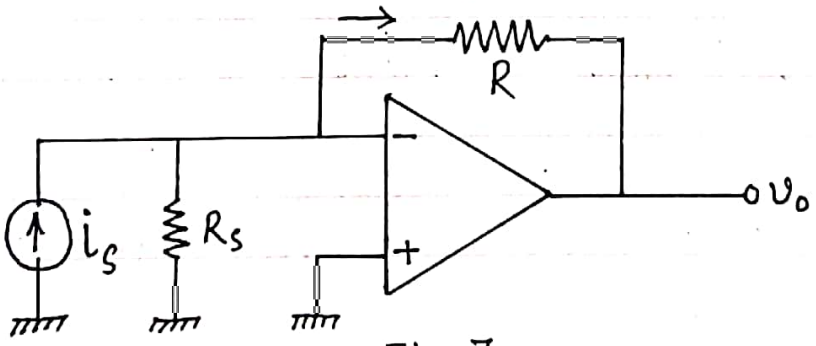


Fig-7

8. Voltage Comparator :

The voltage comparator circuit using op-Amp is shown

in Fig-8. The Comparator can compare two voltages.

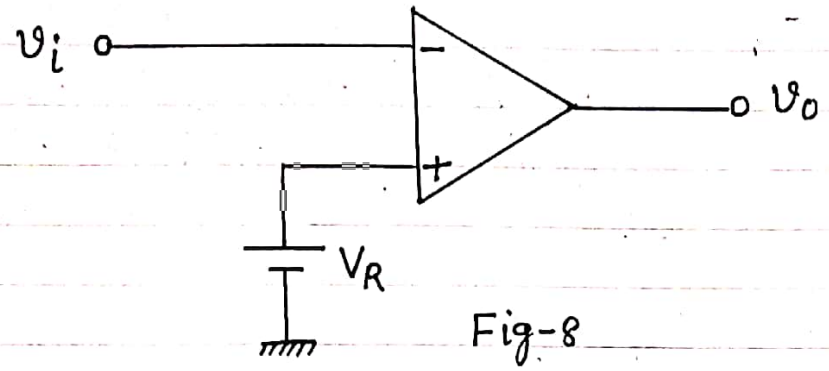


Fig-8

This circuit compares v_i with a reference voltage V_R. As long as $v_i < V_R$, $v_o = +V_{sat}$. As v_i crosses V_R towards the region $v_i > V_R$, $v_o = -V_{sat}$. Thus by looking at the output voltage we can instantly identify whether v_i is greater than or less than V_R. The Comparator circuit can be used to generate a symmetrical square wave from sine wave by taking $V_R = 0$ and v_i as sinusoidal wave.

9. Peak Detector:

The peak detector circuit using op-Amp is shown in Fig-9.

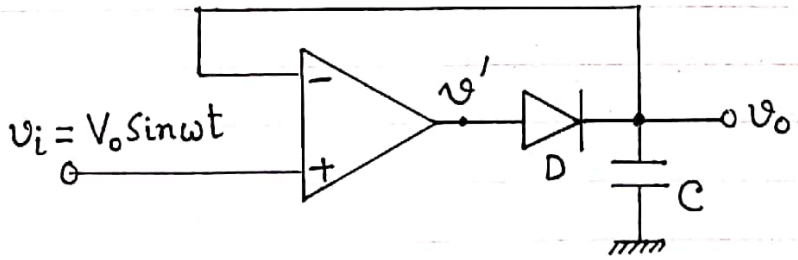


Fig-9

If $v_i > v_o$, the op-Amp output v' is positive saturation. The diode D then Conducts and the capacitor C is charged to the value of input voltage because the gain of the circuit is unity. In this way the capacitor is charged to the

peak value V_o of the input when v_i goes below the capacitor voltage op-Amp output v' becomes negative saturation. The diode then becomes reverse biased and stops conducting. However the capacitor voltage remains at the peak value V_o of the input. Thus the circuit acts as <u>peak detector.</u>

10. Logarithmic Amplifier :

Logarithmic amplifier circuit using op-Amp is shown in Fig-10.

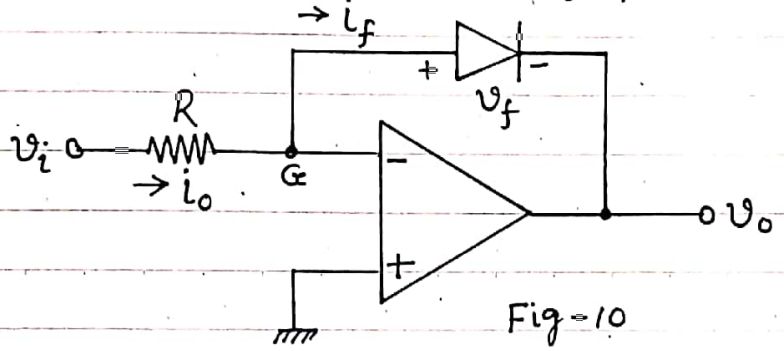


Fig-10

Now $i_o = i_f$

$$\Rightarrow \frac{v_i - 0}{R} = I_s\left(e^{\frac{ev_f}{\eta KT}} - 1\right) \approx I_s e^{\frac{ev_f}{\eta KT}}$$

where I_s is the reverse saturation current of the diode.

$$\therefore \frac{v_i}{I_s R} = e^{\frac{ev_f}{\eta KT}}$$

Taking log on both sides we get

$$\ln\left(\frac{v_i}{I_s R}\right) = \frac{ev_f}{\eta KT} \quad \therefore v_f = \frac{\eta KT}{e} \ln\left(\frac{v_i}{I_s R}\right)$$

The output voltage is $v_o = -v_f = -\frac{\eta KT}{e} \ln\left(\frac{v_i}{I_s R}\right)$

Thus the output voltage is the logarithmic of input voltage

11. Schmitt trigger or regenerative comparator :

The Schmitt trigger circuit using op-Amp is shown in Fig-11. The input voltage v_i is applied to the inverting terminal and the feedback voltage v_f is applied to the non-inverting terminal of op-Amp.

When $v_i < v_f$ the output v_o is at positive saturation level $+V_{sat}$. Then using super-position Theorem we get

$$v_f = \frac{R_2 V_R}{R_1+R_2} + \frac{R_1 V_{sat}}{R_1+R_2} = V_1 \text{ (say)} \quad \text{---(11.1)}$$

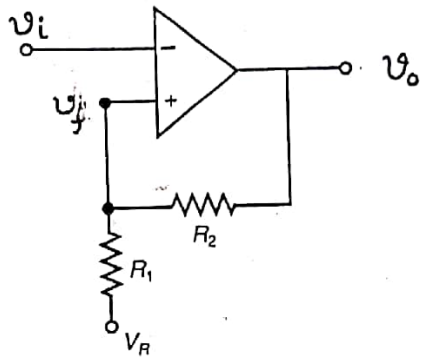


Fig. 11: Schmitt trigger

Let us now increase v_i in the positive direction. Then v_o will remain unchanged at $+V_{sat}$ till v_i attains the threshold, critical or trigger voltage V_1. At this value of v_i, the output v_o of the amplifier switches regeneratively to $-V_{sat}$, the negative saturation voltage. The output is held at $-V_{sat}$ so long as $v_i > V_1$

For $v_i > V_1$ we have

$$v_f = \frac{V_R R_2}{R_1+R_2} - \frac{R_1 V_{sat}}{R_1+R_2} = V_2 \text{ (say)} \quad \text{----(11.2)}$$

If the voltage v_i is now decreased, the output remains at $-V_{sat}$ until $v_i = V_2$. At this voltage the output regeneratively switches to $+V_{sat}$. The complete transfer characteristic is shown in Fig-(11.1)

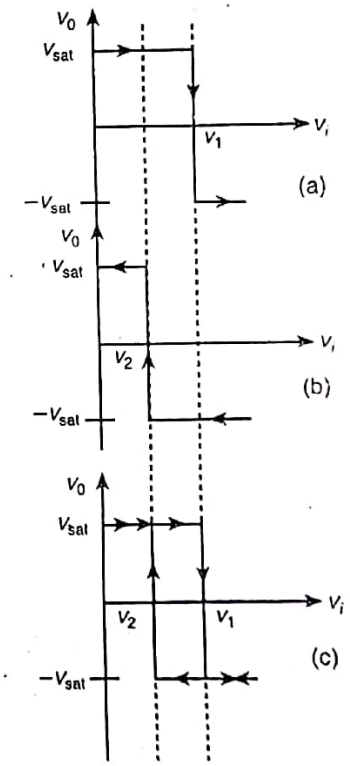


Fig. 11.1 Schmitt trigger (a) transfer characteristic for increasing v_i (b) transfer characteristi for decreasing v_i (c) complete transfe characteristic showing hysteresis

The two input voltages at which the output changes state are called trip points. V_1 is the upper trip point (UTP) and V_2 is the lower trip point (LTP). Thus

$$V_H = V_1 - V_2 = \frac{2R_1}{R_1+R_2} V_{sat} \quad \text{----------(11.3)}$$

V_H is called <u>hysteresis</u>. In order to reduce V_H we have to make $R_1/(R_1+R_2)$ small. But it cannot be reduced greatly, for otherwise the loop gain $-\beta A_V$ becomes small.

Suppose we have to design a Schmitt trigger for which $V_R = 3V$ and $V_H = 0.03\,V$ using op-Amp with $V_{sat} = 5V$ and $A_V = -2\times10^4$. Then

$$V_H = 0.03 = \frac{2R_1}{R_1+R_2} V_{sat} = \frac{10R_1}{R_1+R_2}$$

$$\therefore \frac{R_1}{R_1+R_2} = 0.003$$. The loop gain is $-\frac{A_V R_1}{R_1+R_2} = 60$. This is much larger than 1 and is therefore acceptable. This circuit is used to generate square wave.

12.1. Solution of simultaneous linear algebraic equations :

Let us consider the solution of the following two simultaneous equations

$$a_1x + b_1y = c_1 \quad \ldots\ldots\ldots (12{\cdot}1)$$

$$a_2x + b_2y = c_2 \quad \ldots\ldots\ldots (12{\cdot}2)$$

where a_1, b_1, c_1, a_2, b_2 and c_2 are constants. Solving for the variables x and y we get

$$x = \frac{c_1}{a_1} - \frac{b_1}{a_1}y \quad \ldots\ldots\ldots (12{\cdot}3)$$

$$y = \frac{c_2}{b_2} - \frac{a_2}{b_2}x \quad \ldots\ldots\ldots (12{\cdot}4)$$

These equations can be implemented by using the circuit of Fig. 12.

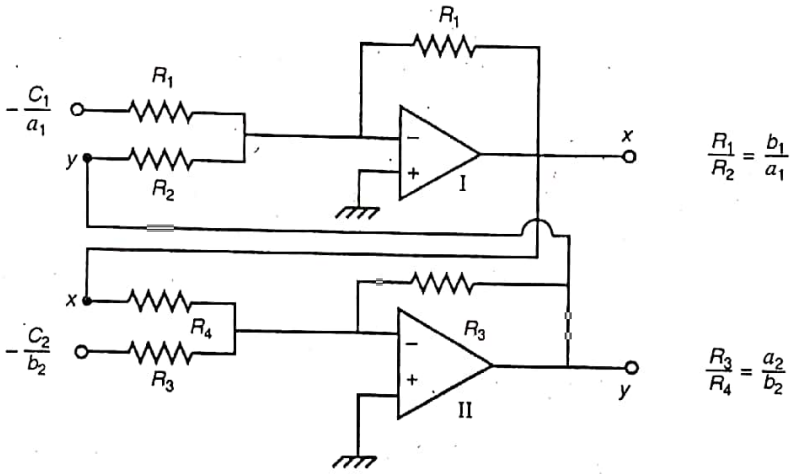


Fig. 12. Solution of algebraic equations

where OP AMPs have been used as adder. Suppose, at first, that $-c_1/a_1$ and y are available as voltages. Then Eq, (12·3) indicates that x can be obtained as the output of a summing amplifier I where $R_1/R_2 = b_1/a_1$. Now Eq. (12·4) indicates that y can be obtained as the output of another summing amplifier II where we assume that $-c_2/b_2$ is available as a voltage and $R_3/R_4 = a_2/b_2$. Once the system is assembled the solutions are immediately obtained in terms of voltages at the output of the two adders. In practical circuits, high resolution potentiometers are used to obtain accurate resistance ratios and input voltages.

13. Solution of differential equation :

Let us consider the solution of the following second order differential equation :

$$\frac{d^2v}{dt^2} + P\frac{dv}{dt} + Qv = v_1 \quad \text{-------(13·1)}$$

where P and Q are real positive constants and v_1 is a given function of time t.

For convenience, let us rewrite Eq. (13·1) as

$$\frac{d^2v}{dt^2} = -P\frac{dv}{dt} - Qv + v_1 \quad \text{- - - - - -(13·2)}$$

To start with let us assume that $\frac{d^2v}{dt^2}$ is available in the form of a voltage.

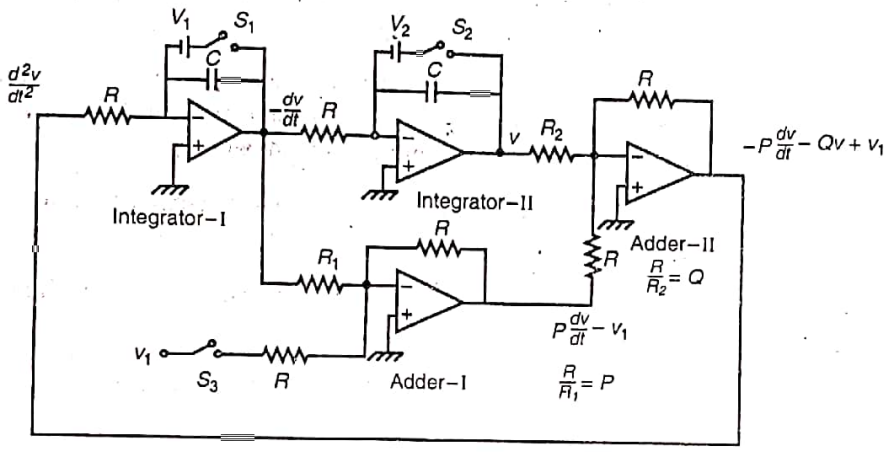


Fig. 13. . Analog computer to solve, the differential Eq. (13·1)

Then at the output of the integrator I in Fig. 13. , a voltage proportional to $-\frac{dv}{dt}$ is obtained. A second integrator II gives a voltage proportional to v.

If the time constants RC of the integrators are chosen as 1s then the output of the integrator I is exactly $-\frac{dv}{dt}$ and that of the integrator II is v.

Now an adder can be constructed whose output will give an output voltage

$$-P\frac{dv}{dt} - Qv + v_1.$$

The output of the integrator I is applied to the input of an adder I. The given function v_1, in the form of a voltage, is also applied to the adder I via a switch S_3. The output of the adder I is thus $p\frac{dv}{dt} - v_1$ where $P = \frac{R}{R_1}$. The output of the adder I and the integrator II are applied to the input of the adder II. The output of adder II thus becomes

$$-P\frac{dv}{dt} + v_1 - Qv$$

where $Q = R/R_2$.

According to Eq. (13.2), this output equals $\frac{d^2v}{dt^2}$ which is the voltage that was assumed to be available at the input terminals. So to complete the analog computer the output of the adder II is connected to the input of the integrator I.

The specified initial conditions i.e., the values of $\frac{dv}{dt}$ and v at $t = 0$ can be inserted into the computer by applying proper d.c. voltages V_1 and V_2 across the capacitors of the integrators I and II.

The solution of the differential Eq. (13.1) can now be obtained at the output of the integrator II with the switches S_1 and S_2 opened and S_3 closed simultaneously by means of a relay at time $t = 0$. The solution may be observed with the help of a cathode-ray oscilloscope (CRO) or may be recorded by means of a recorder.

Here it is important to point but that the above analog computer can be constructed by using differentiators instead of integrators. But integrators are always preferred over differentiators due to the following reasons :

(i) The gain of a differentiator increases with frequency whereas the gain of an integrator decreases with frequency. So it is easier to stabilize an integrator than a differentiator against high frequency spurious signals.

(ii) Because of limited bandwidth, an integrator is less sensitive to noise voltages than a differentiator.

(iii) For a rapidly changing input waveform a differentiator is more likely to be overloaded.

(iv) It is more convenient to insert initial conditions in an integrator.

Problem 6 Compute the voltage gain for the amplifier shown in Fig-6. Find the output voltage v_o if the input voltage is $v_i = 0.5 \sin 100\pi t = 0.5 \sin(2\pi 50t)$.

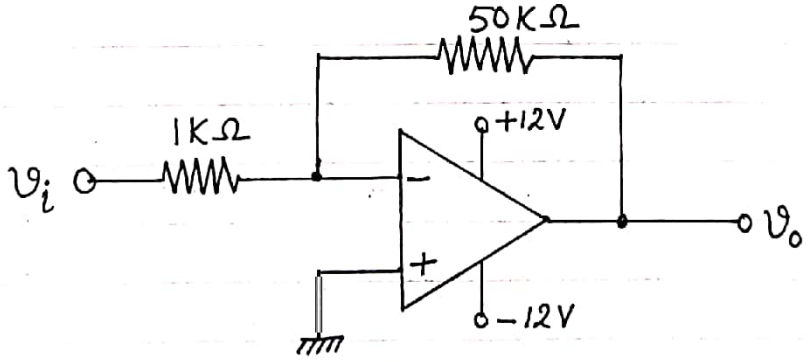


Fig-6.

Solution:

The voltage gain of inverting amplifier (Fig-6) is

$$A = -\frac{50\,K\Omega}{1\,K\Omega} = -50$$

If the operation is entirely linear, the output voltage would have been

$$v_o = Av_i = -50 \times 0.5 \sin 100\pi t$$
$$= -25 \sin 100\pi t \text{ volts}$$

But since the supply voltage is ± 12V, the op-Amp is saturated when $|v_o|$ attains 12V. Let at time $t = t_o$, $v_o = -12$V. Then

$$-12 = -25 \sin 100\pi t_o$$

$$\therefore t_o = \frac{1}{100\pi} \sin^{-1}\left(\frac{12}{25}\right) = 1.59 \times 10^{-3} \text{ sec.}$$

Thus over the complete cycle we have

$v_o = -25 \sin 100\pi t$ volt when $0 \leq t \leq t_o$

$= -12$ volt when $t_o \leq t \leq (0.01 - t_o)$

$= -25 \sin 100\pi t$ when $0.01 - t_o \leq t \leq 0.01 + t_o$

$= +12$V when $0.01 + t_o \leq t \leq 0.02 - t_o$

$= +25 \sin 100\pi t$ Volt when $0.02 - t_o \leq t \leq 0.02$ Sec.

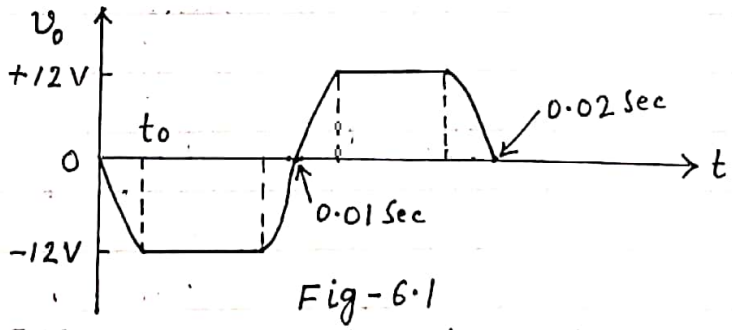


Fig-6.1

The variation v_o with t over a full cycle is shown in Fig-6.1